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PTO/SB/21 (08-03)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	**10/708,056**
Filing Date	**February 5, 2004**
First Named Inventor	**Edmund M. Clarke**
Group Art Unit	**3618**
Examiner Name	
Attorney Docket Number	**361007-000031**

Total Number of Pages in This Submission

ENCLOSURES (check all that apply)

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☒ Information Disclosure Statement
- ☐ Certified Copy of Priority Documents
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to Group ***(Appeal Notice, Brief, Reply Brief)***
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) *(please identify below):*
  **Acknowledgement Postcard*
  **19 cited references*

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual Name	**CHARLES L. MOORE (REG. NO. 33,742)** **MOORE & VAN ALLEN**
Signature	Charles L. Moore
Date	**July 13, 2004**

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Typed or printed name	**Katie M. Efland**		
Signature	Katie M. Efland	Date	July 13, 2004

Attorney Docket: 361007-000031

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Edmund M. Clarke

Group Art Unit:

Serial Number: 10/708,056

Examiner:

Filed: February 5, 2004

For: METHOD AND SYSTEM TO VERIFY A CIRCUIT DESIGN

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. § 1.56 AND 37 C.F.R. § 1.97

It is respectfully requested that the documents listed on the attached Form PTO/SB/08A be considered by the Patent and Trademark Office in the above-referenced application and made of record therein. A full text copy of the relevant documents are enclosed. This information disclosure statement submitted herewith is being filed within three months of the filing date of the application or date of entry into the national stage of an international application or before the mailing date of a first Office action on the merits, whichever event occurs last.

Respectfully submitted,

By: Charles L. Moore

July 13, 2004
Date

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Katie M. Efland

Katie M. Efland

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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 3

Complete if Known	
Application Number	**10/708,056**
Filing Date	**February 5, 2004**
First Named Inventor	**Edmund M. Clarke**
Art Unit	
Examiner Name	
Attorney Docket Number	**361007-000031**

U.S. PATENT DOCUMENTS

Examiner Initials'	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	A	US- 6,131,078		10/10/2000	Plaisted	
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FOREIGN PATENT DOCUMENTS

Examiner Initials'	Cite No.[1]	Foreign Patent Document Country Code[3]–Number[4]–Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

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Substitute for form 1449B/PTO				*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	**10/708,056**
				Filing Date	**February 5, 2004**
				First Named Inventor	**Edmund M. Clarke**
				Art Unit	
(use as many sheets as necessary)				Examiner Name	
Sheet	2	of	3	Attorney Docket Number	**361007-000031**

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	B	Carl Pixley, Guest Editor's Introduction: Formal Verification of Commercial Integrated Circuits. IEEE Design & Test of Computers, 18(4):4-5, 2001.	
	C	Armin Biere, Alessandro Cimatti, Edmund M. Clarke, and Yunshan Yhu. Symbolic model checking without BDDs. In Tools and Algorithms for Construction and Analysis of Systems, pages 193-207, 1999.	
	D	A. Biere, E. Clarke, R. Raimi, and Y. Zhu. Verifying safety properties of a Power PC™ microprocessor using symbolic model checking without BDDs. In N. Halbwachs and D. Peled, editors, Proceedings of the 11th International Conference on Computer Aided Verification (CAB 99), Lecture Notes in Computer Science. Springer Verlag, 1999.	
	E	A. Biere, A.Cimatti, E.M. Clarke, M. Fujita, and Y. Zhu. Symbolic model checking using SAT procedures instead of BDDs. In Design Automation Conference (DAC '99), 1999.	
	F	Joao P. Marques-Silva and Karem A. Sakallah. GRASP – A New Search Algorithm for Satisfiability. In Proceedings of IEEE/ACM International Conference on Computer-Aided Design, pages 220-227, November 1996.	
	G	Matthew W. Moskewicz, Conor F. Madigan, Ying Zhao, Lintao Zhang, and Sharad Malik. Chaff: Engineering an efficient SAT solver. In Proceedings of the 38th Design Automation Conference (DAC '01), June 2001.	
	H	D. Kroening and O. Strichman. Efficient computation of recurrence diameters. In Proceedings of the Fourth International Conference on Verification, Model Checking and Abstract Interpretation. Springer, 2003. To appear.	
	I	O. Shtrichman. Tuning SAT checkers for bounded model checking. In E.A. Emerson and A.P. Sistla, editors, Proceedings of the 12th International Conference on Computer Aided Verification (CAV 2000), Lecture Notes in Computer Science. Springer Verlag, 2000.	
	J	Fady Copty, Limor Fix, Ranan Fraer, Enrico Giunchiglia, Gila Kamhi, Armando Tacchella, and Moshe Y. Vardi. Benefits of bounded model checking at an industrial setting. In Gerard Berry, Hubert Comon, and Alain Finkel, editors, Proceedings of the 13th International Conference on Computer Aided Verification (CAV 2001), number 2102 in Lecture Notes in Computer Science, pages 436-453. Springer Verlag, 2001.	
	K	Per Bjesse, Tim Leonard, and Abdel Mokkedem. Finding bugs in an Alpha microprocessor using satisfiability solvers. In Gerard Berry, Hubert Comon, and Alain Finkel, editors, Proceedings of the 13th International Conference on Computer Aided Verification (CAV 2001), number 2102 in Lecture Notes in Computer Science, pages 454-464. Springer Verlad, 2001.	

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Substitute for form 1449B/PTO **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** *(use as many sheets as necessary)*				***Complete if Known***	
				Application Number	**10/708,056**
				Filing Date	**February 5, 2004**
				First Named Inventor	**Edmund M. Clarke**
				Art Unit	
				Examiner Name	
Sheet	3	of	3	Attorney Docket Number	**361007-000031**

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	L	Luc Semeria, Andrew Seawright, Renu Mehra, Daniel Ng, Arjuna Ekanayake, and Barry Pangrle. RTL C-based methodology for designing and verifying a multi-threaded processor. In Proc. Of the 39th Design Automation Conference ACM Press, 2002.	
	M	I. Page. Constructing Hardware-Software Systems from a Single Description. Journal of VLSI Signal Processing, 1291):87-107, 1996.	
	N	A. Pnueli, M. Siegel, and O. Shtrichman. The code validation tool (CVT) – automatic verification of a compilation process. Int. Journal of Software Tools for Technology Transfer (STTT), 2(2):192-201, 1998.	
	O	R. Cytron, J. Ferrante, B.K. Rosen, M.N. Wegman, and F.K. Zadeck. An efficient method of computing static single assignment form. In Proceedings of the 16th ACM SIGPLAN-SIGACT symposium on Principles of programming languages, pages 25-35. ACM Press, 1989.	
	P	David W. Currie, Alan J. Hu, and Sreeranga Rajan. Automatic formal verification of dsp software. In Proceedings of the 37th Design Automation Conference (DAC 2000), pages 130-135. ACM Press, 2000.	
	Q	Kiyoharu Hamaguchi. Symbolic simulation heuristics for high-level design descriptions with uninterpreted functions. In International Workshop on High-Level Design, Validation, and Test, pages 25-30. IEEE, 2001.	
	R	C. Blank, H. Eveking, J. Levihn, and G. Ritter. Symbolic simulation techniques – state of the art and applications. In International Workshop on High-Level Design, Validation, and Test, pages 45-50. IEEE, 2001.	
	S	Apt., Krzysztof R. Logics and Models of Concurrent Systems, NATO ASI Series, Series F: Computer and System Sciences, Vol. 13.	

Examiner Signature		Date Considered	

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